STRUCTURES AND METHODS FOR DETERMINING THE EFFECTS OF HIGH STRESS CURRENTS ON CONDUCTING LAYERS AND CONTACTS IN INTEGRATED CIRCUITS

ABSTRACT

A test circuit is included in an IC wafer for testing the reliability of ICs under high current stress. The test circuit includes two sensing transistors, a select transistor, and a resistor. The two ends of the resistor are coupled to two sense terminals through the two sensing transistors. One end of the resistor is also coupled to a first stress input terminal; the other end of the resistor is coupled to a second stress input terminal through the select transistor. When the test circuit is selected, the sensing and select transistors are turned on. A current path is formed between the two stress input terminals, and a voltage differential can be measured across the resistor using the two sense terminals. Row and column select circuits enable the rapid testing of many resistor sizes and configurations in an array of such test circuits.